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REMARKS

The Office Action of 08/22/2006 has been carefully considered. Reconsideration and allowance in view of the present remarks is respectfully requested.

Claims 1-10 were rejected as being anticipated by Bauman. The rejection states in part:

[B]auman teaches a device for exchanging data signals between a first clock domain and a second clock..., characterized in that the device comprises a serial memory element [when the registers in the chain are put into a serial shift mode...] and a parallel memory element coupled to the serial memory element, the serial memory element...comprising at least one memory location more for the data signals than the parallel memory element [see Figs. 6A and 6B and related discussion].

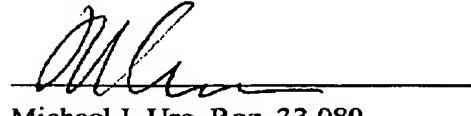
This rejection is respectfully traversed.

Since the same elements are read as being both the serial memory element and the parallel memory element, there is nothing in the reference that would teach or suggest the feature of claim 1 that the serial memory element comprises at least one memory location more for the data signals than the parallel memory element.

Nevertheless, if the Examiner persists in the rejection, Applicant would be willing to amend the claims to recite that the serial memory element and the parallel memory element reside in different clock domains. No such feature is taught or suggested by the cited reference.

Withdrawal of the rejection and allowance of claims 1-10 is respectfully
requested.

Respectfully submitted,



Michael J. Ure, Reg. 33,089

Dated: 11/22/06